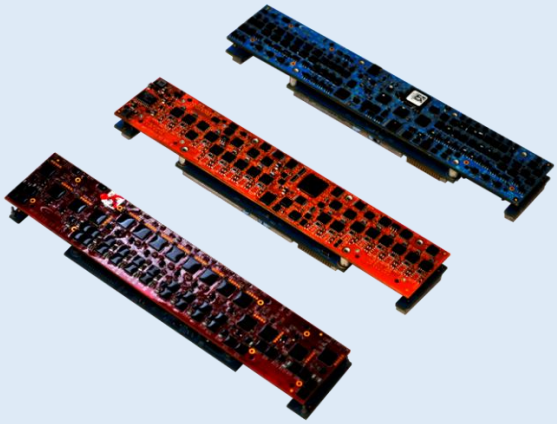
# What are the Advantages of the NAI Function Modules?

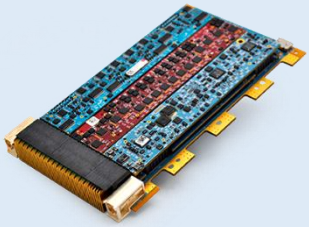
**When Size, Weight and Power are critical NAI provides**

- High funtional denisty
- Wide range of I/O, Commnication, Measurement and Simulation
- Programmable Channels
- Background Built in Test
- ARM processor and FPGA to offload system processor
- TurnKey Solution from one supplier



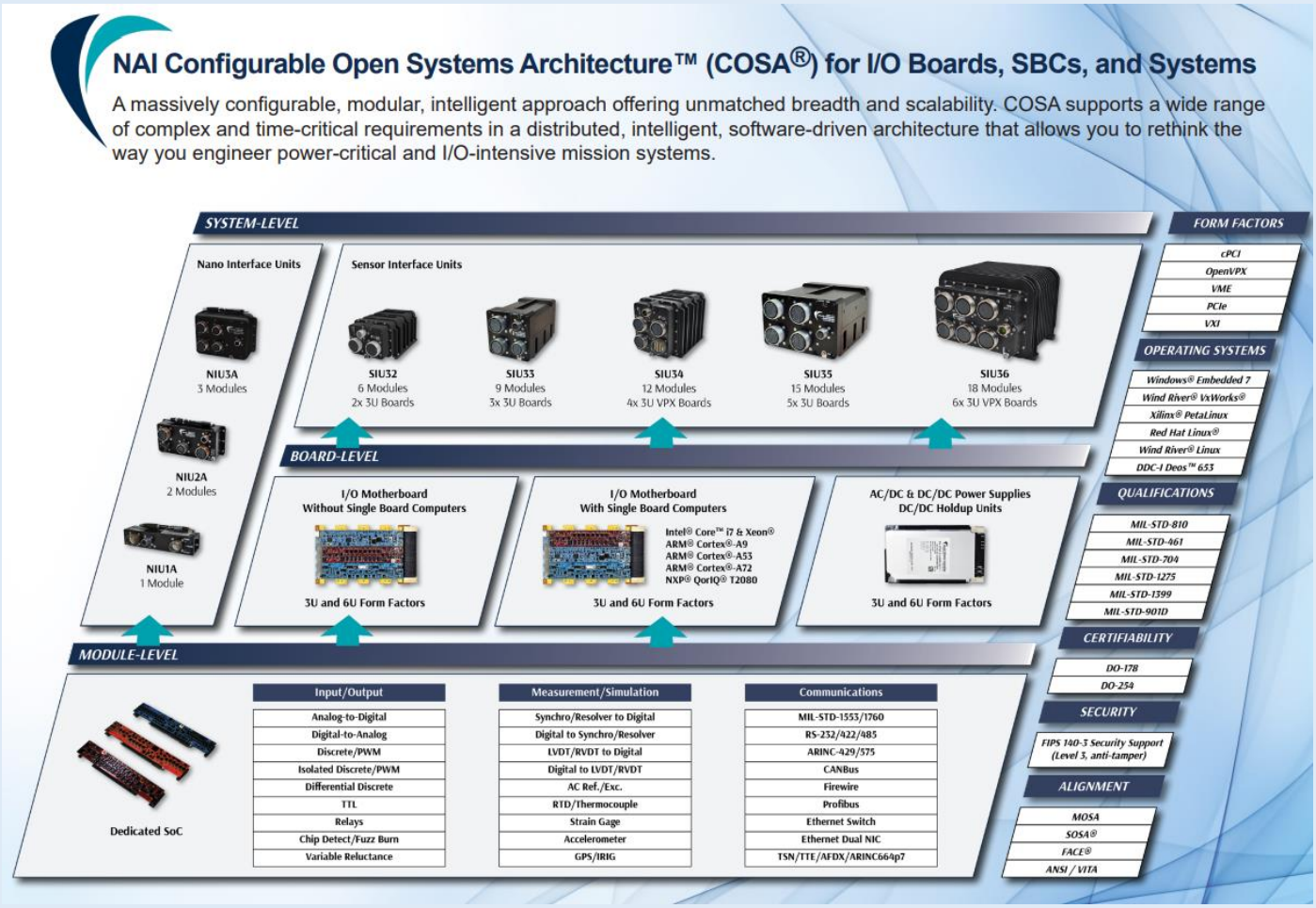
**Over 90 Function Modules Available**
**Board level Products Supported – VPX, VME, cPCI and PCIe and Systems**

**6U VPX/VME – 6 Modules**



**3U VPX – 3 Modules**

**System (3) 3U VPX cards and Power Supply**




**90 Modules Available**

## I/O

- A/D 9 Modules
- D/A 5 Modules
- Discrete I/O 5 Modules
- Digital I/O 2 Modules
- Differntial Tranceivers 2 Modules

## Measurement and Simulation

- LVDT/RVDT 15 Modules
- Synchro/Resolver 26 Modules
- AC Reference 2 Modules
- RDT 3 Modules
- Variable Reluntance 1 Module
- Strain Guage 1 Module

## Communication

- MIL-STD-1553 6 Modules
- ARINC 2 Modules
- Time Triggered Ethernet 1 Module
- IEEE 1394 (FireWire) 2 Modules
- CANBus 3 Modules
- Serial 4 Modules
- Ethernet 1 Module

# I/O Modules

**Analog to Digital –** Analog to Digital (A/D) modules translate analog electrical signals for data processing purposes. NAI offers nine A/D smart function modules. The Adx smart function modules provide fast, accurate and reliable conversion performance ideally suited for military, industrial, and commercial applications. A variety of A/D converters with available channels, architecture type and sampling rates are available to meet your circuit design needs.

| Module | Description |
|---|---|
| AD1 | 12 A/D Channels (±1.25 to ±10.0 VDC FSR); 24-bit Sigma-Delta |
| AD2 | 12 A/D Channels (±100V max); 24-bit Sigma-Delta |
| AD3 | 12 A/D Channels (±25mA FSR); 24-bit Sigma-Delta |
| AD4 | 16 A/D Channels (±1.25 to ±10.0 VDC FSR or ±25 mA) ; 16-bit SAR, 8 Chx2 A/D multiplexed |
| AD5 | 16 A/D Channels (±6.25 to ±50.0 VDC FS); 16-bit SAR, 8 Chx2 A/D multiplexed |
| AD6 | 16 A/D Channels (12.5 to 100.0 VDC FS); 16-bit SAR, 8 Chx2 A/D multiplexed |
| ADE | 16 A/D Channels (±10 VDC); 16-bit SAR per channel |
| ADF | 16 A/D Channels (±100 VDC); 16-bit SAR per channel |
| ADG | 16 A/D Channels (±25 mA); 16-bit SAR per channel |

Modules ADE, ADF and ADG feature 16 channels with 16-bit, individual Successive Approximation Register (SAR) A/D converters for each channel. The maximum programmable, expected full-scale range input for the three modules is ±10 V, ±100 V, and ±25 mA, respectively. The A/D converters have programmable sample rates of up to 200 kSPS max per channel.

Modules ADE, ADF and ADG offer advantages including simultaneous sampling, low power and provide field programmable input range and gain for each channel. All A/D channels are 'self-aligning' with Continuous Background Built-in-Test (CBIT), Initiated BIT (IBIT) and extended off-line diagnostics and status provided for channel health and operation feedback. Each channel includes a fixed, second-order, anti-aliasing input filter and a digital, second-order IIR low-pass output filter with a programmable break frequency that enables users to field-adjust the filtering for each channel. The modules also include extended A/D FIFO buffering capabilities for greater storage/management of the incoming signal samples (data) for post processing applications. Programmable FIFO buffer thresholds maximize data flow control (in and out of the FIFO).

Taking advantage of the fast and simultaneous sampling SAR A/D architecture, the module provides an effective A/D interface for applications requiring control loop integration and parallel data acquisition. The A/D Module Threshold, Saturation and Measurement registers can be programmed to be utilized as an IEEE 754 single-precision floating-point value or as a 32-bit integer value. Applications include control loops, data acquisition, synchronous data across channels and additional Programming (thresholds, floating point, etc.)

"The addition of ADE, ADF and ADG smart modules expands our COSA® Architecture aligning with MOSA, SOSA and FACE." states Lino Massafra, VP of Sales and Marketing. "These new modules expand the flexibility, adaptability and modularity offered by our portfolio of board and system level products."

**Features**

- The input range is field programmable for each channel.
- Each channel includes an anti-aliasing filter and a low-pass filter with a programmable breakpoint.
- All channels have continuous background Built-In-Test (BIT).
- The module(s) also include extended A/D FIFO buffering capabilities for greater storage/management of the incoming samples for post processing applications

**Built-In Test (BIT)/Diagnostic Capability**
Three different tests, one online (D2) and two off-line (D0, D3), can be selected:
The online (D2) test initiates automatic background BIT testing, where each channel is checked to a test accuracy of 0.2% FS. Any failure triggers an Interrupt (if enabled) with the results available in BIT status register. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus. In addition, all channels are monitored for open input.

The off-line (D3) test starts an initiated BIT test that disconnects all A/D's from the I/O and then connects them across an internal stimulus. Each channel will be checked to a test accuracy of 0.2% FS. Test cycle is completed within 20 seconds and results can be read from the Status registers when D3 changes from 1 to 0. The test can be stopped at any time and requires no user programming. It can be enabled or disabled via the bus. A/D Open Circuit monitoring is disabled during D3 testing.

An off-line (D0) test is used to check the card and interface. Write 1 to D0 of Test Enable register to disconnect all A/D channels from the I/O and to connect them across an internal D/A. Test parameters are controlled by the user and are entered in the D0 Test Voltage and D0 Test Range registers. The outputs from the A/D channels are compared to the internal D/A for proper conversion. External reference voltage is not required.

**Digital to Analog –** Digital to Analog (D/A) modules convert digital electrical signals to an analog signal. NAI offers for D/A smart function modules offering from four (high voltage) to sixteen output channels. The Dax smart function modules also include D/A FIFO buffering for greater control of the output voltage and signal data. Once enabled and triggered, the D/A FIFO buffer accepts, stores, and outputs the voltage (and/or current) commands for applications requiring simulation of waveform generation (single or periodic).

| Module | Description |
|---|---|
| DA1 | 12 D/A Outputs (±10 VDC or ±25 mA) |
| DA2 | 16 D/A Outputs (+10 VDC or +10 mA) |
| DA3 | 4 (High Current) D/A Outputs (±40 VDC or +100 mA) |
| DA4 | 4 (High Voltage) D/A Outputs (+20 VDC to +80 VDC) |
| DA5 | 4 High-Voltage/High-Current (External VCC) D/A Outputs |

**Features**
- High-quality D/A conversion, 16-Bit/channel
- Continuous background BIT
- External trigger/synchronization
- Automatic shutdown protection with the results displayed in a status word
- Extended D/A FIFO buffering capabilities

**Built-In Test (BIT)/Diagnostic Capability**
Two different tests, one online (D2) and one offline (D3), may be selected:

The online (D2) test initiates automatic background BIT testing, where each channel is checked to a test accuracy of 0.2% FS and monitored for shorted output. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

The offline (D3) test uses an internal A/D that measures all D/A channels while they remain connected to the I/O and cycle through a number of signal levels. Each channel will be checked to a test accuracy of 0.2% FS. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from 1 to 0. The test can be stopped at any time. This test requires no user programming and can be enabled or disabled via the bus.

**Discrete I/O –** Discrete I/O multichannel programmable modules provide interfacing solutions for almost any embedded or test application. NAI's discrete I/O modules are offered in two versions: Standard Functionality (SF) modules and Enhanced Functionality (EF) modules. All the modules feature unparalleled programming flexibility, a wide range of operating characteristics, and a unique design that eliminates the need for pull-up resistors or mechanical jumpers. The EF Modules add built-in operational functionality to provide Pulse/Frequency Period Measurements of the incoming signal (Input) and/or Pulse/Frequency arbitrary signal generation (Output).

| Module | Description |
|---|---|
| DT1 | 24 Ch , Discrete I/O (0 to 60 VDC, 500 mA/Ch.) |
| DT2 | 16 Discrete/Switch I/O Channels (±80 V, 625 mA/Ch.) |
| DT3 | 4 Discrete/Switch I/O Channels (±100 V, 3 A/Ch.) |
| DT4 | Enhanced 24 Discrete I/O Channels (0 to 60 VDC, 500 mA/Ch.) |
| DT5 | Enhanced 16 Discrete/Switch I/O Channels (±80 V, 625 mA/Ch.) |

**Features**

- 24 channels available as inputs or outputs
- Programmable for Input (voltage or contact sensing) or Output (current source, sink or push-pull) per channel/bank
- Programmable debounce circuitry with selectable time delay eliminates false signals resulting from relay contact bounce
- Built-in test runs in background constantly monitoring system health for each channel
- Ability to sense broken input connection and if input is shorted to +V or to ground
- Ability to read I/O voltage and output current for improved diagnostics (indicates if load is connected)

**Automatic Background Built-In Test (BIT)/Diagnostic Capability**

The Discrete module supports automatic background BIT testing that verifies channel processing. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of the module. This capability is accomplished by an additional test comparator that is incorporated into each module. The test comparator checks each channel and is compared against the operational channel. Depending upon the configuration, the Input data read, or Output logic written of the operational channel and test comparator must agree or a fault is indicated with the results available in the associated status register. The results of the tests are stored in the BIT Dynamic Status and BIT Latched Status registers.

The technique used by the continuous background BIT (CBIT) test consists of an "add-2, subtract-1" counting scheme. The BIT counter is incremented by 2 when a BIT-fault is detected and decremented by 1 when there is no BIT fault detected and the BIT counter is greater than 0. When the BIT counter exceeds the (programmed) Background BIT Threshold value, the specific channel's fault bit in the BIT status register will be set. Note, the interval at which BIT is performed is dependent and differs between module types. Rather than specifying the BIT Threshold as a "count", the BIT Threshold is specified as a time in milliseconds. The module will convert the time specified to the BIT Threshold "count" based on the BIT interval for that module. The "add-2, subtract-1" counting scheme effectively filters momentary or intermittent anomalies by allowing them to "come and go" before a BIT fault status or indication is flagged (e.g. BIT faults would register when sustained; i.e. at a ten second interval, not a 10-millisecond interval). This prevents spurious faults from registering valid such as those caused by EMI and/or dirty power causing false BIT faults. Putting more "weight" on errors ("add-2") and less "weight" on subsequent passing results (subtract-1) will result in a BIT failure indication even if a channel "oscillates" between a pass and fail state.

In addition to BIT, the Discrete module tests for overcurrent conditions and provides Above Max High Threshold, Below Min Low Threshold, and Mid-Range statuses for threshold signal transitioning.

**Digital I/O TTL and CMOS –** TTL offers high switching speed and relative immunity to noisy systems. CMOS sensors provide image sensing technology by converting light waves into signals that are small bursts of current. These waves can be light or other electromagnetic radiation. NAI's TTL/CMOS Modules are offered in two versions: our Standard Functionality (SF) an Enhanced Functionality (EF) module. The transistor-transistor logic (TTL) employs transmitters with multiple emitters in gates having more than one input.

| Module | Description |
|---|---|
| TL1 | 24 TTL Channels, Programmable I/O |
| TL2 | 24 TTL Channels, Enhanced, Programmable I/O |

**Features**

- 24 channels available as inputs or outputs
- Programmable debounce circuitry with selectable time delay eliminates false signals resulting from relay contact bounce
- Built-in test runs in background constantly monitoring system health for each channel

**Automatic Background Built-In Test (BIT)/Diagnostic Capability**

These modules contain automatic background BIT testing that verifies channel processing (data read or write logic), tests for overcurrent conditions and provides status for threshold signal transitioning. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It continually checks that each channel is functional. This capability is accomplished by an additional test comparator that is incorporated into each module. The test comparator checks each channel and is compared against the operational channel. Depending upon the configuration, the Input data read or Output logic written of the operational channel and test comparator must agree or a fault is indicated with the results available in the associated status register. Low-to-High and High-to-Low logic transitions are indicated.

There is no independent overcurrent detection. Instead, the BIT detection circuitry is used to infer an overcurrent condition if the output state setting doesn't match the readback value seen by the input circuitry. For example, a shorted output, causing the read state to be opposite from the expected value would trigger this. If the fault persists beyond the BIT interval stabilization time, the overcurrent protection will kick in and reset the drive output by returning the transceiver to input mode. To reset this condition, a reset command needs to be issued to the Overcurrent Clear register, which will restore drive output and allow the latched status to be reset. This is separate from the reset for the Interrupt Enable Overcurrent register on this module. It is recommended that a reset command is done whenever status is cleared to avoid a non-apparent output reset condition

**Differential Transceivers -** Differential transceivers increase resistance to noise by creating two complementary signals. These complementary signals produced on balanced lines double noise immunity by creating lower power requirements due to lower supply voltages. NAI's modules are offered in two versions: the Standard Functionality (SF) module and the Enhanced Functionality (EF) module. Both modules feature 16 individual RS422/RS485 I/O channels that are programmable for either input or output, and include extensive diagnostics.

| Module | Description |
|---|---|
| DF1 | 16 Differential I/O Multi-Mode Transceiver Channels |
| DF2 | Enhanced 16 Differential I/O Multi-Mode Transceiver Channels |

**Features**

- 16 channels available as inputs or outputs
- Programmable for fast or slow slew rates
- Programmable debounce circuitry with selectable time delay eliminates false signals resulting from relay contact bounce (pending)
- Built-in test runs in background constantly monitoring system health for each channel.

**Automatic Background Built-In Test (BIT)/Diagnostic Capability**

These modules contain automatic background BIT testing that verifies channel processing (data read or write logic), tests for overcurrent conditions and provides status for threshold signal transitioning.
Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled via the bus (see further details in register description), and continually checks that each channel is

functional. This capability is accomplished by an additional test comparator that is incorporated into each module. The test comparator checks each channel and is compared against the operational channel. Depending upon the configuration, the Input data read or Output logic written of the operational channel and test comparator must agree or a fault is indicated with the results available in the associated status register. Low-to-High and High-to-Low logic transitions are indicated.

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